1.0.ACD

1.1 REQUIREMENTS FOR ACD AND SUMMARY OF ACCOMPLISHMENTS

The Anti-Coincidence Detector (ACD) is designed to reject the majority of charged particles, which are the background for any gamma-ray experiments. The ACD of EGRET has suffered from the self-veto effect when the products of the high energy photon interactions in the instrument's calorimeter cause a veto signal in ACD (backsplash effect), resulting in the significant degradation of the efficiency for high energy (> 5 GeV) gamma rays. To avoid this effect, the ACD for GLAST is designed to be subdivided into many scintillating tiles with waveshifting fiber readout.

In GLAST, the requirements for background rejection and rate control are system-wide requirements and all subsystems play a role. In determining the requirements for the ACD, we need to understand the various fluxes involved and the functional approach to triggering GLAST. We pointed out that for studies of photons, eliminating the electron background, not the proton background, is the dominant and driving requirement for the ACD-tracker combination because the calorimeter cannot distinguish between them. The scientific requirement that drives the instrumental background rejection requirement is the study of the diffuse high-latitude background. We need to separate the contribution from point sources and find out if there is any residual diffuse emission. We require that the background due to charged particles be less than 10% of this signal.

We spent considerable effort in validating the background intensities (Ormes et al. 1999) and including the effects of albedo fluxes from the atmosphere. We set the GLAST system level design requirements for the misidentification of charged cosmic rays to be 3×10^{-5} or a detection efficiency of 0.99997. The electron component drives the requirement for ACD to have **0.9997 efficiency.** We can expect one "9" from the top tracker layer to meet our requirement.

The ACD subsystem has had modest funding during the technology development phase. This decision was based on the minimal need for development work in this area. Nevertheless, we have accomplished a number of things during this technology development phase.

- Analyzed 1997 beam test data and determined the relationship of backsplash signals to ACD panel size, distance from calorimeter, electronics threshold, and energy dependence of response so that flight design could be specified.
- Exposed the paddles built for the 1997 beam test to a higher energy beam at CERN and measured backsplash at higher energies up to 300 GeV.
- Developed specifications for flight unit electronics.
- Built 13 paddle ACD units for the beam test engineering model (BTEM) with electronics fabricated to flight-like specifications built with commercial parts.
- Delivered BTEM/ACD to SLAC and supported beam test. All electronics and hardware functioned as specified and preliminary results are included with this report.
- Conducted simulations of instrument response to determine optimal arrangement and sizing
 of ACD tiles to minimize background, enable ACD to be included into trigger and
 determined its impact on trigger rates.
- Conducted simulations of the rejection of electrons by the ACD, especially with respect to the objective of searching for gamma-ray lines using events whose trajectory intercepts a

- large path length in the calorimeter. These events will have the best energy resolution for energies > 50 GeV where lines are most likely to be found.
- Based on the above, arrived at a configuration for the flight unit ACD, developed resource requirements (e.g. volume, mass, power, cost) to build it, and determined its power to reject background and control event rates.

1.2 Flight Anticoincidence Detector (ACD) Development Plan

The ACD will be designed, fabricated and tested at GSFC. It is the only GLAST subsystem that is not modular, so it will be delivered to SLAC for integration as a unit. Table 1.1 lists the parts and materials needed in its construction. The assembly procedure is outlined below, based on methods already used for fabrication of the ACD for the upcoming beam test:

- Complete the design of ACD within allocated mass (175kg + 54 kg reserve) and electrical power (29W + 26W reserve) budgets.
- Fabricate support structure, including attachment points for scintillators and phototubes (PMT). Because the ACD is a large structure, a full-scale mechanical model will be constructed and tested at GSFC (vibration and acoustics).
- Purchase scintillator tiles with grooves. Bond waveshifting fibers into grooves and gather
 into bundles for attachment to PMT. Wrap tiles and fibers with Tyvek and light barrier, then
 attach fibers to PMT interface. Connect PMT power and signal cables to prototype power
 converters and electronics. Test all assemblies using ground-level cosmic rays and laboratory
 sources
- Develop and test ASIC for front end electronics, FPGA for digital logic.
- Attach tile/fiber/PMT assemblies to the support structure, using Velcro and carbon fiber ribbons. Wire cable harness for all PMTs to power supplies/electronics. Attach thermal blanket/micrometeoroid shield. Conduct full performance test before delivery to SLAC, using sources and cosmic rays.

Table 2.3.2.7 ACD Parts and Fabrication.

| Element | Parts & materials | Fabrication & Assembly |
|----------------------|-------------------------|--|
| Scintillators/Fibers | Bicron 408 scintillator | Bicron subcontractor cuts high-quality grooves for |
| | Bicron 91A/MC | embedding the fibers into the scintillators. |
| | waveshifting fibers | GSFC LHEA bonds the fibers. |
| Wrapping | Tyvek | Tyvek for light reflection, opaque layer to isolate tiles in |
| | Opaque wrap (TBD) | case of penetration by micrometeoroid. |
| Phototubes | Hamamatsu R1635 or | Magnetic shielding. Hamamatsu can build bases with |
| | R5611, space-qualified | voltage divider or Cockroft-Walton HV supplies, potted |
| | tubes | for vacuum. |
| HV | Hamamatsu HV supply or | Purchase as part of phototube assembly or build from |
| | Cockroft-Walton | design used for EGRET phototubes. |
| | converters | |
| Front-end ASIC and | Custom design by GSFC | Process TBD, based on best available; design by GSFC |
| related electronics | | group doing Swift MIDEX and analog design for beam |
| | | test tower. |
| FPGA logic | Actel | Common buy for all subsystems; programming by GSFC |
| | | engineer based on beam test experience. |
| Support Structure | Composite, low-density, | Goddard Mechanical Engineering/Composites group |
| | high-strength | design, parts manufactured by local contractor, assembly |
| | Space-qualified rigid | by GSFC in-house. |
| | foam for spacing | |
| Outer Shielding | Nextel ceramic fabric | High-strength fabric bumper layers, as used on the |
| (thermal and | | International Space Station (ISS). |
| micrometeoroid | Solimide foam | Low-density, flexible foam for spacers, used on Shuttle. |
| protection) | Kevlar | Backing shield, good penetration resistance. |
| | MLI | GSFC blanket group will handle assembly, similar to the |
| | | EGRET blanket. |

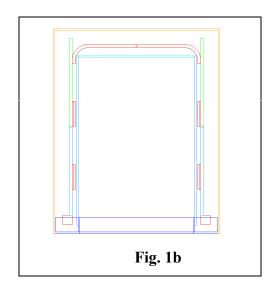
1.3. ACD DEVELOPMENT STATUS

1.3.1 ACD Status/Description

A scaled-down version of the flight ACD was developed and delivered according to schedule to the SLAC facilities for the December 1999 beam-test. The delivery of the beam-test ACD was the culmination of an integrated development plan that took the results of the simulations and trade studies performed in the basic period of the contract, plus our previous experience with charged particle and gamma-ray detectors, to develop our baseline ACD design concept. The main components (detector, mechanical, electrical, and software) of the beam-test ACD were conducted in parallel. The ACD components were integrated and tested together as a complete subsystem in a bench/laboratory environment before delivery to SLAC. Functional and performance/characterization tests of the ACD were performed during this integration and test period.

The beam-test ACD consists of the main ACD "hat" structure and the ACD Electronics Cardcage assembly. The beam-test ACD "hat" was designed to fit over the one-tower beam-test prototype implementation of the Tracker/Calorimeter assembly. The ACD electronics box was designed to be mounted external to the ACD "hat" and to be connected via a short electrical harness to the detectors and signal processing electronics located inside the ACD "hat". Fig.1 has pictures of the completed system; a) shows the assembled "hat", b) is a schematic view of ACD, and c) is a photo of one electronic board. A more detailed description of the beam-test implementation follows.

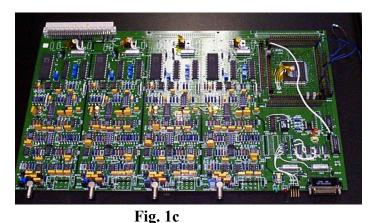




In order to assist the flight design, the beam-test design has a combination of flight-like details that will be used to mimic as close as possible the proposed flight design and different experimental configurations. That will explore different detailed implementation options. This includes selecting and using flight qualified materials, mounting tiles that closely resemble the expected flight configuration, and placing PMTs under the tiles and elsewhere to determine where best to place them for flight.

1.3.1.1. ACD Detector Design/Development

The beam-test ACD used plastic scintillator tiles as the charged particle detector for the subsystem. Each tile is read out using a set of wave-shifting fibers (embedded into the tiles) that are connected to a Photo-Multiplier Tube (PMT). A total of 12 scintillator tiles, four on the top and 2 on each side,



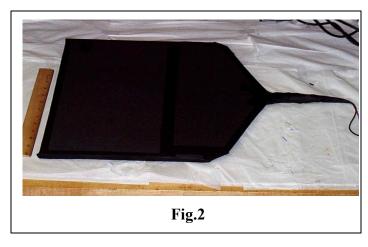
were mounted to the main mechanical structure (hat) of the ACD. The PMTs of the side tiles are located underneath the tiles, while the PMTs for the top tiles are located underneath the upper side tile (fig. 1b).

The eight side tiles were all designed and manufactured as flat tiles, while the four tiles on the top were designed and manufactured with a bend/curve. The curved tiles allow us to "seal" the corners of the detector against charged particle leakage. The manufacturing of bent/curved tiles for this application was new, therefore the tiles were procured as early as possible to minimize unforeseen problems with this new process. The company Bicron, which has extensive experience producing plastic scintillators of the type we needed, manufactured the tiles. Bicron also machined the grooves for the wave-shifting fibers into the tiles. This decision helped to save us time and money. All the work with the tiles was done by one company, minimizing the problems and paperwork. In addition, this provided the additional benefits of having the machining done by a company that had extensive experience machining plastic scintillator, thus ensuring that our cleanliness and polish requirements would be met. The flat, grooved tiles were delivered without much problems in the beginning of June 1999, however, Bicron did encounter some difficulties manufacturing the bent, curved tiles. The problems were solved and they were delivered at the end of July 1999, about 2 months late. This did not affect the ACD schedule due to the early procurement of the tiles. Assembly of the flat tiles with the fibers and PMTs proceeded in parallel.

The PMTs and the wave-shifting fibers were all received by the end of March 1999. The PMT used for the beam-test was the Hamamatsu R-1635. All PMTs were tested and characterized upon their arrival.

The assembly of the tile/fiber/PMT subassemblies began once the flat tiles were delivered in June 1999. All tiles had their wave-shifting fibers glued into their grooves and each tile was wrapped with two layers of light-reflecting TYVEC paper, and one layer of black paper (for light isolation). The PMT was then attached to the tile/fiber subassembly

(Fig.2). All tile/fiber/PMT subassemblies were completed by the beginning of September and each subassembly was tested initially with laboratory test equipment. All subassemblies were subsequently tested and characterized with one channel of the beam-test Front-End-Electronics (FEE) boards to determine their effective gain, efficiency, noise and uniformity of response.



1.3.1.2. ACD Mechanical Design/Development

A mechanical subassembly was designed and developed to allow mounting of all tile/fiber/PMT subassemblies and to permit it to fit snugly over the top of the tracker/calorimeter subsystems. The beam-test mechanical subassembly does not extend below the Simulated Grid Top; the ACD covers the majority of the tracker portion of the tower only. The mechanical subassembly consists of two main components: the support structure and the channel frame assembly.

The mechanical support structure is made out of 1/16" thick aluminum. It consists of a 380mm by 380mm by 540mm(h) box that was manufactured using sheet metal construction methods and whose surfaces were black anodized. The mechanical channel frame assembly was machined out of a single piece of aluminum and was also black anodized. The channel frame assembly attaches to the bottom of the support structure and contains helicoil inserts that allow it to be attached via bolts to the designated interface points of the beam-test simulated grid top.

The mechanical interfaces between the ACD and the beam-test tower were established early in the development, before initiating the detailed design of the ACD mechanical components. Interface drawings were exchanged, reviewed and approved between GSFC and SLAC. A mechanical template with the locations of the bolt holes was sent to SLAC before the delivery of the ACD to ensure the interfaces were correct. Once the interfaces and mechanical requirements had been finalized, the detailed design and manufacturing of the mechanical components began. The mechanical components were completed on schedule at the end of April 1999. At this point they were delivered for integration and mounting of the detectors and "hat" electronics. The support structure was used for optimum layout of the tiles/fibers/PMTs and the electrical harnesses. The channel frame assembly was used to determine the placement of all Pre-Amp printed circuit boards (PCBs), connectors, trim potentiometers, and internal harnesses located inside the channel. Once the location of all these channel components had been established, holes and cutouts were made to the channel frame assembly to allow placement of all connectors and trim-potentiometers.

1.3.1.3. ACD Electronics Design/Development

The ACD beam-test electronics consists of two main sections: the main FEE boards and the Pre-Amp boards. The Pre-Amp boards are a set of twelve small PCBs that fit into the channel frame assembly and interface directly with each of the twelve PMTs located underneath the plastic scintillator tiles. An electrical harness connects the preamplifier boards directly to the signal processing circuits on the main FEE boards. The electrical harness also provides the ACD "hat" with the high voltage needed for the PMTs and the power necessary for all internal "hat" electronics.

The main FEE boards are located inside a VME cardcage that is mounted externally to the beam-test prototype tower. Each FEE board contains four analog signal processing channels that allow it to process the signals from 4 separate PMT/Pre-Amps. Each analog processing chain contains two main discriminator circuits (one that corresponds to minimum ionizing particle (*mip*) and the other for heavy ions) and a Pulse Height Analysis (PHA) circuit. In addition, each FEE board is controlled by one Atmel Field Programmable Gate Array (FPGA) which contains all the digital control logic needed to control each analog channel individually and provides the necessary interface logic and protocol needed to communicate with the TEM-ACD board. Various Digital-to-Analog Converters (DACs) are used in each analog channel for programmable threshold set points and programmable high voltage settings. These DACs are controlled via the FPGA and can be reprogrammed by sending a command to the FEE board via the TEM-ACD board. Analog and digital housekeeping circuits are also present on each FEE board to allow monitoring of key channel and board parameters (Fig.1c).

A common design and PCB layout was used for all FEE boards. All the boards are identical except for special jumper settings used to identify each board. This modular PCB design proved advantageous because it provided cost and times savings due to the fact that only one PCB layout was necessary. In addition it facilitated testing because the same test procedure used to test the first board was used to test each additional board. The use of the Atmel FPGA also proved to be beneficial due to its reprogrammable nature, which allowed us to make logic modifications to the board after the FPGA had been soldered onto the board. Seven FEE boards were manufactured and populated allowing us to process and control not only the 12 detectors present on the ACD "hat" but also various stand-alone detector subassemblies used for testing purposes during the beam runs.

The FEE boards were tested using the TEM-ACD subsystem delivered to GSFC at the end of June 1999. Special software was developed to run with the Vx-Works operating system used by the TEM-ACD board and the ground station computers. The latter were used to send commands and collect all science and housekeeping date from the beam-test ACD electronics. Integration and testing of the first FEE board with the TEM-ACD subsystem took place during the months of July and August. This included functional testing of the complete FEE board in addition to characterization and performance tests for each analog channel of the board. The integration and testing of the remaining 6 FEE boards occurred during the months of September and October. During this time an easier-

to-use graphical user interface (GUI) software was developed to send commands and view histograms of the PHA data.

The FEE electronics were integrated to the completed ACD "hat" assembly and a complete end-to-end test, which also included the TEM-ACD board and the ground station computers took place during the month of November 1999. At this point a new, updated TEM-ACD board was delivered to GSFC. New electrical harnesses were fabricated to accommodate the new MDM connectors of the updated TEM-ACD board. New software was generated to interface and control the additional features of the new TEM-ACD board. The board was subsequently integrated and tested with the complete ACD subsystem at this time.

1.4. SUMMARY OF MEASUREMENTS AND LABORATORY DEVELOPMENTS

1.4.1 MEASUREMENTS USING BREADBOARD DESIGNS

We have spent considerable time analyzing and understanding the results of the 1997 SLAC beam test, verifying the efficiency measurements in the laboratory and extending the backsplash measurements to the top of the GLAST energy range.

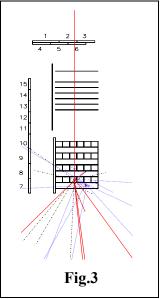
The goals of these tests were the following:

- verification of the choice of wave shifting fibers for light collection
- study of angular distribution and energy spectrum of backsplash
- measurement of the ACD efficiency for electrons (minimum ionizing particles)
- test use of 2 layers
- validation of extrapolation of backsplash to higher energies

Two sets of scintillating paddles read out by waveshifting fibers were designed and built for the 1997 SLAC beam test. The results and detectors are described in detail elsewhere (Atwood et al. 2000). The first module was placed on the side of the tracker/calorimeter tower, and the second one upstream of the tower in the beam. By identifying the incident particles, carefully counting them and then examining those detector paddles outside of the beam, we could measure detector efficiency, the probability of an event of given energy producing a backsplash signal and the backsplash energy deposited. Efficiency measurements were also carried out in the laboratory using cosmic ray mouns. Monte Carlo GEANT codes and GLASTSIM runs were created and compared for the beam test configuration and results.

To extend the backsplash measurements the instrumental hardware used in SLAC'97 beam test was refurbished and exposed in the proton/electron beam at CERN in June, 1999. The approach and experimental setup were very similar to the SLAC'97 beam test.

a) **Backsplash measurements:** A high energy (> 5 GeV) photon/electron initiated shower in a calorimeter produces a large number of soft photons some of which may penetrate through the calorimeter and other material and produce signals in the anticoincidence detector through the Compton scattering. For EGRET this effect resulted in ~50% efficiency degradation at 10 GeV, relatively to 1 GeV. The experimental setup for the measurement of backsplash from the test calorimeter at



x 10 ⁻³ 0.45 Backsplash per degree[^] 0.4 a) 0.35 0.25 0.2 0.15 0.05 100 120 140 160 180 Direction on the tile, degrees Fig.4

SLAC ('97) is shown in Fig. 3. The measured fraction of events accompanied by backsplash above 0.2× mip (energy loss of a minimum ionizing particle) is shown in Fig. 4 for different direction on the scintillating tile, and for energy of photons of 20 GeV. A similar setup was used at CERN in the summer of 1999. The fraction of events with backsplash above different discriminator thresholds for the energy range from SLAC energies (5 GeV) to CERN

energies (300 GeV) are presented in Fig. 5.

- b) **Efficiency:** The measured efficiency of electron detection as a function of discriminator threshold (in the units of mean *mip* energy loss) is shown in Fig. 6. It was measured using both the electron beam at SLAC (filled circles) and in the laboratory using cosmic ray muons (open circles). Unidentified background in the beam could have degraded the measured efficiency, so we believe that the presented values of the efficiency are conservative. They agree with estimates based on photoelectron statistics and indicate the detection of 30 photoelectrons for a minimum ionizing particle (mip) traversing the detector with normal incidence. These measurements are consistent with the pulse height distribution widths made with the BTEM paddles built this year.
- c) Configuration studies: Various investigations were also conducted to study and determine the most effective way to collect the light from the scintillator tiles. Waveshifting bars (WSB) and direct-coupled PMTs were considered as alternatives to the baselined wave-shifting fibers (WSF). Laboratory tests were conducted to compare

their light collection responses. The test results conclude that the WSF provide much better uniformity of response and that it is still the best choice. Laboratory tests were also conducted to measure the WSF readout sensitivity area. These tests were in support of a concept of segmenting the ACD based on how groups of fiber are

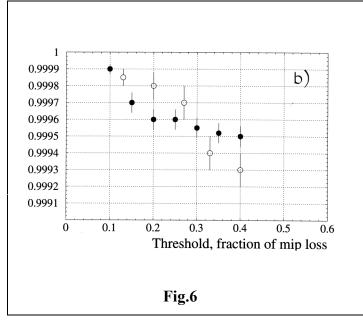
bundled instead of physically having separate ACD tiles. The results show that concept would not work because the fibers are sensitive to a distance of up to 10-15 cm from their edge.

As a result of this work we determined that:

- a) An efficiency of more than 0.9995 for single charged minimum ionizing particles (mip) is achievable without problems, with discriminator setting of >15-20% of a mip. This discriminator threshold avoids any problems from noise and reduces the backsplash effect.
- b) The angular distribution of backsplash has a broad minimum of $\pm 60^{\circ}$ around backward direction, in agreement with the models for electromagnetic shower development in high Z (atomic number) materials.
- c) GEANT and GLASTSIM simulations, performed for the beam test configuration, predict less backsplash than measured in beam test. We have used the beam test

Backsplash in 144 sq. cm tile at 45 cm from calorimeter Fraction of events with backsplash reshold 0.2 mig 10 Energy, GeV with backsplash threshold 0.3 mig 10 Fraction of events 10 Energy, GeV Fraction of events with backsplash threshold 0.4 mip 10 10 10 Energy, GeV Fig.5

results to make probabilities estimates of self-veto. We determined that additional

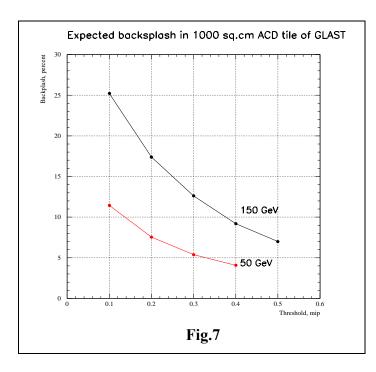


- measurements at higher energy are needed for the self-veto prediction at energies up to 300 GeV.
- d) The two laver design gave a factor of only 2-3 reduction in the self-veto. We determined that a single layer is adequate and optimal because the m u c h more complicated 2-laver design would require significant additional mass and budget.

e)These data

allowed us to determine an empirical formula to calculate the backsplash above a given discriminator threshold in a tile of any area placed at different distances from the calorimeter for the given incident photon/electron energy and in various orientations. We have sized the ACD tiles on the top of the GLAST tracker to be $\cup 1000 \text{ cm}^2$ so that the relative efficiency for this instrument will be degraded by no more than 20% at 300 GeV, the highest energy accessible to GLAST, as per specification (Fig. 7).

1.4.2 1999 SLAC beam test.



The major effort of the past year has been the development of a higher fidelity ACD that can simulate flight like performance and test the design concepts. The concepts were developed as described in the previous section. They have been implemented for the 1999 beam test unit, known as the GLAST BTEM. The goals for the ACD portion of the technology development effort were:

Primary goals:

a) verify ACD design – physics, mechanics, electronics b) verify simulations of the ACD design – efficiency,

leakage, backsplash avoidance

c) test and validate DAQ interface design concepts

Secondary goals:

- a) study possible high-voltage electromagnetic interference with other components
- b) study bending, routing, and mounting of wave-shifting fibers
- c) test attachment of scintillators to structure
- d) test methods of building light-tight housings

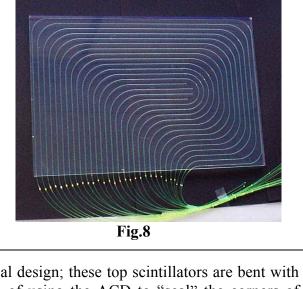
Knowing that we wish to validate the performance of a GLAST tower and DAQ on a balloon flight, we designed the BTEM/ACD so that it could be flown on a balloon with minimum modification. The design concept and a photo of the BTEM/ACD before

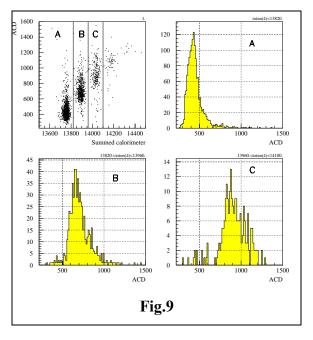
integration to the remainder of the system was shown earlier in Fig. 1.

The BTEM/ACD design can be summarized as follows

- a) ACD is a separate unit (aka a "hat") that covers the tracker part of the tower.
- b) All scintillating tiles (12 in total) are viewed by Hamamatsu R1635 phototubes through multicladding BC-91MC wave-shifting fibers.
- c) Top ACD is divided into four tiles with some gaps in between with the goal to study the efficiency
 - degradation around possible gaps in real design; these top scintillators are bent with embedded fibers solving the problem of using the ACD to "seal" the corners of GLAST against charged particles.
- d) Some PMTs are hidden under side scintillators, others are not so that the impact of cascades from the calorimeter hitting the PMTs can be evaluated.
- e) Lower side tiles have a curved fiber groove pattern designed to minimize the distance to the PMT (Fig. 8). This is to test the design for flight when we will have very limited space for the fibers and PMT accommodation on the bottom of ACD.

Preliminary tests showed that all the tiles worked as expected. Fig.9 presents the data collected in 5 GeV electron run: the left upper panel shows the ACD pulse-height vs. the calorimeter summed pulse-height. Events with 1, 2, 3 and 4 particles are clearly separated. The ACD data applying calorimeter selections are shown in right upper panel (1-particle events are selected), in left lower panel (2-particle events) and in right lower panel (3 particle events). Variation of the resolution with signal obtained is consistent with about 36 photoelectrons, indicating the expected improvement in light collection over the earlier units. Detailed analysis of the collected experimental data is in process.

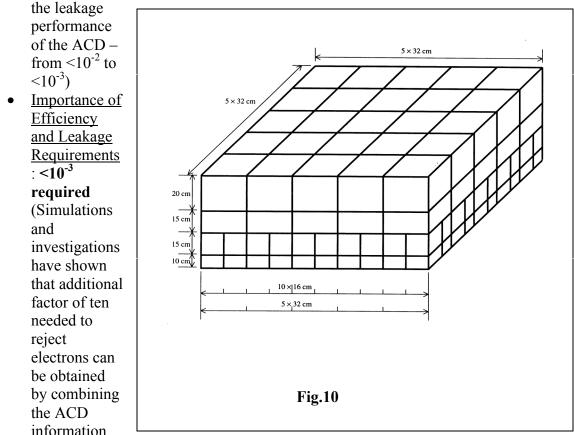




1.4.3 Flight ACD trade study and design.

Combining the extensive Monte Carlo simulations and and the beam and laboratory test results completed during this period allowed us to define the flight unit ACD specifications and requirements. Most of the simulations have to do with the overall configuration of the plastic scintillator tiles. Some of the simulations/investigations and their results are summarized below:

- <u>ACD tile area required</u>: ~1000cm² (On top. For the sides, specification varies with distance of tile from calorimeter and is science driven.)
- <u>1 tile layer vs. 2 tile layers (on top)</u>: **1 Layer is Acceptable** (Charged particle detector efficiency requirement can be met with only 1 layer and certain gap size between adjacent tiles)
- <u>Gap Width</u>: **<2mm gap, overlap of tiles is desirable** (Simulations show that the efficiency requirements are marginally met for this gap width and provide a conservative number for fabrication of the "hat".)
- <u>Tile gap alignment with respect to Towers</u>: **Misalignment recommended** (Simulations have shown that misaligning the tile gaps with the tower gaps improves



The simulation and modeling effort will continue to study the design margin and different failure modes of the present design configuration and to see if a less conservative design can still meet background rejection requirements.

with tracker information.)

These studies and measurements combined with the scientific goals for GLAST and the background rejection requirements demonstrate that the following design specifications for the GLAST ACD can be met:

- a) ACD must be >0.9997 efficient to the singly charged minimum ionizing particles and have leakage $< 3 \times 10^{-4}$. This drives the requirement for photoelectrons from the tile and its light collecting system, the thickness of scintillator, the fiber frequency and placement, and uniformity of response.
- b) Efficiency degradation due to backsplash-caused self-veto should be not more than 20% over the entire energy range up to 300 GeV. If this requirement is met at 300 GeV, it can be met at all lower energies.
- c) Redundancy needs to be carefully considered. All critical elements are currently designed to be redundant. The failure of a single tile would cause 10-15% increase in the trigger rate after application of the ACD.
- d) Optimized footprint of GLAST dictates very limited room for the ACD on the sides; design studies and laboratory models show that this can be less than 5cm (excluding thermal blanket).
- e) Resistance of the ACD to accidental puncture by a micrometeoroid requires each tile to be independently enclosed and light tight. The possibility to do this is an important motivation for our choice of the tiling structure of the ACD.
- f) Unique possibility to detect high energy gamma-ray lines, possibly originating from dark matter annihilation, would be improved if we use off-angles events with long paths in the calorimeter and consequently better energy resolution. These trajectories typically have shorter paths from ACD to the calorimeter. We have set the sizes of the tiles on the tracker sides to maintain the self-veto at the level of <20% at 300 GeV.

We meet these requirements with the design shown in Fig. 10. It is a single layered ACD with a total of 145 separate tiles. Each tile is viewed by 2 redundant PMT through two separate wave-shifting fibers sets. All tiles are overlapped to eliminate the gaps between them. The goal is to seal all gaps by bending tiles at the corners (a capability proven during the fabrication of the BTEM/ACD) and by overlapping tiles.

In the process of conducting these tests and developing the BTEM/ACD, we have developed a set of electronics specifications for the flight unit. They are presented in DRAFT form in Appendix.

REFERENCES:

- 1. J.F.Ormes et al. Report on Rates, 1999, GLAST website
- 2. 2. W.Atwood et al. NIM 2000, in press

APPENDIX A.I: ACD ELECTRONICS REQUIREMENTS

1.2.1 Purpose of the ACD Electronics

1.2.1.1 Primary -

The primary function of the GLAST ACD electronics is to deliver a logic signal to the data acquisition system (DAQ) when a minimum ionizing particle (MIP) hits one of the scintillator tiles.

1.2.1.2 Secondary (must not interfere with primary function) –

The secondary function of the electronics is to deliver a logic signal to the DAQ when a highly-ionizing particle (Carbon, Nitrogen, or Oxygen nucleus) hits one of the scintillator tiles.

1.2.1.3 Tertiary (must not interfere with other functions) –

The third function of the electronics is to deliver a pulse height analysis (PHA) signal to the DAQ for each tile with a MIP signal, upon receipt of a Level 1 Trigger (L1T) signal from the DAQ.

1.2.2 Background Information

The ACD signals are generated as follows:

A MIP hitting a 1 cm thick plastic scintillator tile deposits ~2 MeV, which appears in the form of optical light (~21,000 photons with peak wavelength 425 nm).

The light is absorbed by wavelength-shifting fibers embedded in the scintillator and then re-radiated at a wavelength of 490 nm.

A fraction of this light is trapped in the fibers and carried by total internal reflection to a photomultiplier tube (PMT).

The photocathode converts the light to electrons, ~35 electrons for a MIP.

With a gain of 1 x 10^6 , the phototube produces 35 x 10^6 electrons in a short pulse (< 10 ns). This is equivalent to about 6 picoCoulombs (pC). Averaged over 10 ns, this is 0.6 milliAmps (mA), which produces a signal of 30 milliVolts (mV) in a 50Ω resistance. Typical rate of MIPs in each of the scintillator tiles is 1 KHz.

1.2.3 Descriptions of Functional Elements

1.2.3.1 Preamplifier

The PMT signal is used for three different functions. The preamplifier converts the charge signal to a voltage signal that is easily divided for the three paths. It reduces the capacitive loading on the PMT.

Output: voltage proportional to input charge; voltage range as needed for discriminators and PHA; width and timing jitter as needed to meet overall timing requirement.

1.2.3.2 VETO Circuit for MIPs – Primary Function of ACD

This is the primary function of the ACD, allowing veto of incident charged particles. **Discriminator**

Input: voltage signal from preamplifier

Outputs: (1) logic signal, 0-5V; width <50 ns; latency and timing jitter to meet overall trigger timing requirement. For test purposes, the signal width can be longer, but the beam test, balloon flight, and flight versions should all have short signals.

FPGA (Field Programmable Gate Array)

All discriminator signals feed into one FPGA in the single ACD electronics box.

Input: 0-5V logic signal from discriminator

L1T Logic: FPGA forms logic signals for "tower" based on MIPs seen in tiles nearest each tower.

L1T Output: one VETO logic signal sent by hard wire to each tower if a MIP is seen in a tile associated with that tower.

Timing: the VETO logic signal for the L1T must arrive at the tower TEM no more than TBD nsec after the initial MIP passage. The nominal value for this has been carried as 110 nsec, as follows:

| Scintillator response | 2 nsec |
|-----------------------|--------|
| Waveshifter fibers | 12 |
| Phototube | 9 |
| Preamp/discrim/FPGA | 80 |
| Cable propagation | 7 |

The requirement is that the VETO signal arrive before the L1T from the tracker or calorimeter. The minimum time for these the tracker or calorimeter signals has not yet been defined. We need to know if this timing requirement produces a significant impact on the power of the electronics, compared to a value of 200 nsec or more.

The VETO signal should not arrive at the tower TEM less than TBD nsec after the initial MIP passage. The current value for this is 50 nsec. We may want to tighten up this range of timing values for the flight unit.

Level 2 and 3 Trigger (L2T and L3T) VETO signal

Logic: the FPGA passes the MIP signals for each tile to the DAQ after receipt of a L1T signal.

1.2.3.3 HIREQ Circuit for High-Ionizing Particles (CNO Nuclei) – Secondary Function of the ACD Electronics

This signal provides a trigger to the calorimeter when a heavy nucleus has hit, allowing calibration of the calorimeter.

Discriminator

Input: voltage signal from preamplifier

Output: logic signal, 0-5V; width <50 ns; timing to meet overall trigger timing requirement.

FPGA (Field Programmable Gate Array)

HIREQ Trigger signal Logic: FPGA forms logic signals for "tower" based on High-Ionizing signals seen in tiles nearest each tower.

Output: one HIREQ logic signal sent by hard wire to each tower if a High-Ionizing signal is seen in a tile associated with that tower.

Timing:

The requirement is that the HIREQ signal arrive before the calorimeter signal is formed.

Logic: the FPGA passes the HIREQ signals for each tile to the DAQ after receipt of a L1T signal.

1.2.3.4 Pulse Height Analysis (PHA) – Tertiary Function of the ACD Electronics

Rationale – this signal provides diagnostic information about the operation of the ACD. **Peak Shaper**

Input: voltage signal from preamplifier

Output: shaped voltage signal, with height proportional to peak of input signal voltage.

Pulse Height Analyzer (Analog to Digital Converter, ADC)

Input: shaped voltage signal from peak shaper

Trigger to digitize signal: MIP signal from L1T discriminator or L1T from DAQ (TBD

which)

Output: digitized pulse height value (channel)

FPGA (Field Programmable Gate Array)

All digital signals feed through one FPGA in the single ACD electronics box. This is a different FPGA from the one that handles the trigger signals.

Input: digitized PHA value

L1T trigger

Logic: FPGA formats PHA values for a given L1T Output: PHA values transferred to DAQ by IDB

Timing: time tag or other signal needed in order to identify the event.

1.2.3.5 Other Functions of the ACD Electronics

Commands

High voltage for PMTs – format TBD

Threshold setting for VETO discriminator. A Digital to Analog Converter (DAC) is needed.

Threshold setting for HIREQ discriminator. A Digital to Analog Converter (DAC) is needed.

Gain setting for PHA – if needed?

Housekeeping Data

The following values should be read out periodically:

HV setting for PMT

Temperatures at selected locations